REMARKS

In the present application, claims 1-20 are pending. Claims 1-20 are rejected. Claims 1, 9, 16, 17 and 19 have been amended. Claims 21-24 have been added. No new matter has been added. Claims 2, 10 and 18 are canceled. As a result of this response, claims 1, 3-9, and 11-17, and 19-24 are believed to be in condition for allowance.

Claim Rejections – 35 USC § 103

The Examiner rejected claims 1-3, 5-11, and 13-14 as being unpatentable over Earnest ('338) in view of Sato ('149).

With respect to claim 1, the Examiner asserts that a combination of the teachings of Earnest and Sato, such a combination being neither suggested nor recommended by the Applicants, recites the elements of claim 1. While taking no position on the correctness of the Examiner's assertion, Applicants respectfully assert that claim 1 as amended herein presently recites elements which are neither taught nor suggested by either Earnest or Sato, taken alone or in combination.

Claim 1 is amended herein to read (in relevant part):

> an allocator and control unit programmable by said CPU for specifying individual ones of buffer locations and buffer sizes within said single dual port memory for individual ones of said channel interfaces, and for enabling individual ones of said buffers, said allocator having outputs coupled to said address generator for controlling the generation of addresses thereby depending on which channel interface is currently selected for access to said single dual port memory **wherein in a first case said control unit operates individual ones of channel buffers in a block access mode of operation using a set of channel registers and in a second case said control unit operates said individual ones of channel buffers in a first in/first out (FIFO) access mode of operation using said same set of channel registers.** (emphasis added)

Antecedent basis for the amendment may be found in the specification at page 6, line 27 to page 7, line 4 wherein there is described the operation of the channel registers. As the Examiner concedes, when discussing grounds for rejection with regards to claim 2, "Earnest

does not disclose operating channel buffers [in] a block access mode ...", and as Sato makes no mention of a "block access mode", Applicants respectfully submit that claim 1, as amended, is distinguishable from the prior art and is in condition for allowance.

However, as claim 1 is amended, in part, to include elements of claim 2 (now canceled), specifically the operation of the channel buffers "in one of a block access mode and in a first in/first out (FIFO) access mode of operation", there follows an examination of the Examiner's rejection of the subject matter of claim 2.

With respect to claim 2, the Examiner asserted that "Earnest does not disclose operating channel buffers [in] a block access mode ...", but that Ngai [('635)] discloses operating a section of memory in block access mode ...". While taking no position on the correctness of such an assertion or the permissibility of such a combination, Applicants respectfully maintain that neither Earnest nor Ngai, taken alone or in combination, teach or suggest controlling the operation of individual channel buffers in a block access mode using a set of registers **and** a FIFO mode "**using said same set of channel registers**".

Claim 1 now recites that the operation of individual channel buffers proceeds in one of two modes wherein the same "set of channel registers" controls the operation in either mode. The Examiner implicitly concedes the novelty of this element when asserting the rejection of claim 18. Claim 18 recites, in relevant part, "where when operating in the FIFO Mode said register BaseReg1 functions as a Low Threshold Register and said register SizeReg1 functions as a High Threshold Register." The Examiner allows that Earnest does not specifically show "SizeReg1 as a High Threshold Register ... However, Earnest does show generating ... an FULL flag indicating a High Threshold Register being used." Without taking a position on the teachings of Earnest, the Examiner's interpretation of Earnest is not equivalent to the recitations of claim 1. A flag, which must occupy its own location in memory, that indicates the status of a register as "FULL" is substantively different from a single "set of registers" which may themselves be utilized, in FIFO mode, to store threshold information. In short, claim 1 now recites the novel use of a single "set of channel registers" operated to control two different modes of operation.

It is therefore evident that the art cited by the Examiner fails to teach or suggest, alone or in combination, the element of operating "individual ones of channel buffers in one of a block access mode and in a first in/first out (FIFO) access mode of operation using a set of

channel registers". Applicants therefore traverse the Examiner's rejection of claim 1. The cancellation of claim 2 renders the Examiner's rejection of claim 2 moot. As claims 3-8 depend upon claim 1, claims 3-8 are likewise in condition for allowance.

Claim 9 has likewise been amended to recite "a set of channel registers" and "using said set of channel registers to operate individual ones of channel buffers in a block access mode or a first in/first out (FIFO) access mode of operation." For the reasons discussed above, claim 9 is in condition for allowance. The cancellation of claim 10 renders the Examiner's rejection of claim 10 moot. As claims 11-14 depend upon claim 1, claims 11-14 are likewise in condition for allowance.

Claim 15 has been similarly amended to recite "using a set of channel registers". For the reasons discussed above, claim 15 is in condition for allowance. As claim 16 depends upon claim 15, claim 15 is likewise in condition for allowance.

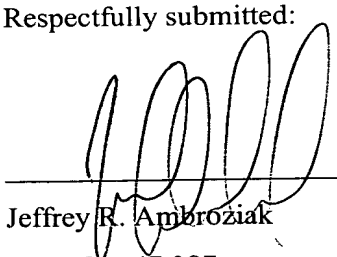
Claim 17 has been amended to recite the elements of claim 18. As discussed above in response to the Examiner's rejection of claim 18, Earnest teaches a separate flag for storing a FULL flag and does not teach the use of a register as claimed. Claim 17 is therefore in condition for allowance.

Lastly, claim 19 has been amended to recite "wherein a set of channel registers controls the operation in said block mode and in said FIFO mode." For the reasons discussed above, claim 19 is in condition for allowance. As claim 20 depends upon claim 19, claim 20 is likewise in condition for allowance.

An earnest and thorough attempt has been made by the undersigned to resolve the outstanding issues in this case and place same in condition for allowance. If the Examiner has any questions or feels that a telephone or personal interview would be helpful in resolving any outstanding issues which remain in this application after consideration of this amendment, the Examiner is courteously invited to telephone the undersigned and the same would be gratefully appreciated.

It is submitted that the claims herein patentably define over the art relied on by the Examiner and early allowance of same is courteously solicited.

Respectfully submitted:



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